

Fpga Spice A Simulation Based Power Estimation Framework

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FPGA-SPICE: A Simulation-Based Architecture Evaluation ...

In this paper, we develop a simulation-based architecture evaluation framework for FPGAs, called FPGA-SPICE, which is released to the public [13]. FPGA-SPICE enables full-chip-level layout estimation and electrical simulations of FPGA architectures, which eases area and power studies. Being tightly integrated within the popular academic architecture

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In this paper, we introduce a simulation-based power estimation framework for FPGAs, called FPGA-SPICE, which supports any FPGA architecture that can be described with an architectural description...

(PDF) FPGA-SPICE: A simulation-based power estimation ...

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FPGA-SPICE: A simulation-based power estimation framework ...

FPGA-SPICE is a simulation-based tool dedicated to accurate power estimation of Field Programmable Gate Arrays (FPGAs)¹. FPGA-SPICE is an extension to the Verilog-To-Routing (VTR) tool suite² and is tightly integrated into the Versatile Placement and Routing (VPR) tool. FPGA-SPICE aims at generating SPICE netlists of a wide range of FPGA architectures, enabling accurate power analysis.

FPGA-SPICE – LSI - EPFL

FPGA-SPICE: A Simulation-based Power Estimation Framework for FPGAs Tang, Xifan ; Gaillardon, Pierre-Emmanuel ; De Micheli, Giovanni Mainstream Field Programmable Gate Array (FPGA) power estimation tools are based on probabilistic activity estimation and analytical power models.

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simulation-based power estimation framework for FPGAs, called FPGA-SPICE, which supports any FPGA architecture that can be described with an architectural description language. Our power estimation engine automatically generates accurate SPICE netlists according to the FPGA configurations and enables precise power analysis of FPGA architectures.

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Simulation Program With Integrated Circuit Emphasis (SPICE) Field Programmable Gate Array (FPGA) Very Large Instruction Word (VLIW) SPICE Simulator FPGA Architecture These keywords were added by machine and not by the authors. This process is experimental and the keywords may be updated as the learning algorithm improves.

Accelerating the SPICE Circuit Simulator Using an FPGA: A ...

FPGA-SPICE: A simulation-based power estimation framework for FPGAs. Share on. Authors: Xifan Tang. Integrated Systems Laboratory (LSI), École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Vaud, Switzerland .

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Simulation acceleration techniques have been around for about two decades, but most products are based on FPGAs from one or two leading FPGA vendors. Usually, it does not matter which FPGA family is used on the simulation acceleration board if the design is coded using synthesizable RTL. However, growing design complexity, along with shrinking ...

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A SPICE simulation is an iterative numerical computation that consists of a device model evaluation phase, a tricky matrix factorization phase and a sequential control phase that drives the numerical integration and linearization phases.

Enhancing Speedups for FPGA Accelerated SPICE through ...

X. Tang, P. Gaillardon, and G. De Micheli. Fpga-spice: a simulation-based power estimation framework for fpgas. In 2015 33rd IEEE International Conference on Computer Design (ICCD), volume, 696–703. Oct 2015.

Publications & References — OpenFPGA 1.0 documentation

Why OpenFPGA?¶ OpenFPGA aims to be an open-source framework that enables rapid prototyping of customizable FPGA architectures. As shown in Fig. 1, a

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conventional approach will take a large group of experienced engineers more than one year to achieve production-ready layout and associated CAD tools. In fact, most of the engineering efforts are spent on manual layouts and developing ad-hoc CAD ...

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Simulation acceleration techniques have been around for about two decades, but most products are based on FPGAs from one or two leading FPGA vendors. Usually, it does not matter which FPGA family is used on the simulation acceleration board if the design is coded using synthesizable RTL. However, growing design complexity, along with shrinking ...

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